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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,746	07/24/2003	Hatsuki Kanbayashi	115816	8139

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,746	KANBAYASHI, HATSUKI	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 01142004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 4, 6, 9, 10, 13, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Masayuki et al. (US 6,693,346 B2).

3. Regarding Claim 1, Masayuki et al. disclose a method of manufacturing a semiconductor device, comprising:

mounting a semiconductor chip (4C) (Figure 5) having electrodes (at 6) on a substrate (base plate) having wiring patterns (connection terminals) (1B), and

forming conductive layers ("strata on a surface") (5D,5F) that electrically connect the electrodes and the wiring patterns in a manner to pass side surfaces of the semiconductor chip.

4. Regarding Claims 2, 4,and 10, Masakuki et al. disclose (See Figure 5) (bottom) that the chips are bonded "face-up."

5. Regarding Claim 3, Masayuki et al. disclose a method of manufacturing a semiconductor device, comprising:

stacking in layers a plurality of semiconductor chips (4C,4D,4F) having electrodes (at 6) on a substrate (1) having wiring patterns (1A), and

forming a conductive layer (5C,5D,5F) that electrically connects the electrodes of any one of the semiconductor chips and the wiring patterns in a manner to pass a side surface of at least one of the semiconductor chips.

6. Regarding Claim 6, Masayuki et al. disclose forming a second conductive layer (right side, right hand equivalent of left hand 5C,5D,5F) that electrically connects the electrodes (at 6) of one of the semiconductor chips and the electrodes (at 6) of another of the semiconductor chips in a manner to pass a side surface of at least one of the semiconductor chips.

7. Regarding Claim 9, Masayuki et al. disclose a semiconductor device, comprising:

a substrate (base plate) (1) (Figure 5) having wiring patterns (1B),

a plurality of stacked semiconductor chips (4C,4D,4F) having electrodes (at 6),

a conductive layer (5C,5D,5F) that electrically connects the electrodes of any one of the semiconductor chips and the wiring patterns in a manner to pass a side surface of at least one of the semiconductor chips, and

a second conductive layer (right side,right hand equivalent of left hand 5C,5D,5F) that electrically connects the electrodes (at 6) of one of the semiconductor chips and the elec-

trodes (at 6) of another of the semiconductor chips in a manner to pass a side surface of at least one of the semiconductor chips.

8. Regarding Claim 13, Masayuki et al. disclose (Figure 18) (Col. 11, lines 28 – 48) a circuit assembly on a substrate (209) (Figure 21(a)) with the semiconductor device mounted therein.

9. Regarding Claim 14, Masayuki et al. do not explicitly disclose a piece of electronic equipment where the device would be used, but it is inherent that the device would be utilized in a piece of electronic equipment, including any application where memory devices are required, for example, a personal computer.

Claim Rejections – 35 U.S.C. 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 5, 7, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masayuki et al., as applied to Claims 1 – 4, 6, 9, 10, 13, and 14, and further in view of Yang (US 6,291,881 B1).

12. Regarding Claim 5, Masayuki et al. do not disclose a method wherein a second semiconductor chip is mounted that is smaller than a first semiconductor chip among the plurality of semiconductor chips being mounted on the first semiconductor chip. Yang discloses mounting a smaller semiconductor chip (404b) (Figure 4B) on the first semiconductor chip (402) with the conductive layer (400) attached (electrically) to electrodes. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Yang in attaching the smaller chip to the larger chip using a resin or paste, in Masayuki et al. to provide a rigidly mounted device configuration.

13. Regarding Claim 7, Masayuki et al. do not disclose a method that includes "face-down" bonding of a first semiconductor chip among the plurality of semiconductor chips to the substrate, and "face-up" bonding of a second semiconductor chip to a side of the first semiconducor chip opposite to a side where the electrodes are formed. Yang discloses (Figure 4A) face-down bonding of the first chip (402) and an attachment at the opposite face of second chip, 404A, using resin or paste, wherein the second chip is bonded face-up. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Yang in attaching the second chip to the first chip using a resin or paste, in Masayuki et al. to provide a rigidly mounted device configuration.

14. Regarding Claim 11, Masayuki et al. do not disclose a device, wherein a second semiconductor chip is mounted that is smaller than a first semiconductor chip among the plurality of semiconductor chips being mounted on the first semiconductor chip. Yang

discloses mounting a smaller semiconductor chip (404b) (Figure 4B) on the first semiconductor chip (402) with the conductive layer (400) attached (electrically) to electrodes. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the device structure of Yang, wherein the smaller chip is attached to the larger chip using a resin or paste in Masayuki et al. to provide a rigidly mounted device configuration.

15. Regarding Claim 12, Masayuki et al. do not disclose a device that includes "face-down" bonding of a first semiconductor chip among the plurality of semiconductor chips to the substrate, and "face-up" bonding of a second semiconductor chip to a side of the first semiconducor chip opposite to a side where the electrodes are formed. Yang discloses (Figure 4A) face-down bonding of the first chip (402) and an attachment at the opposite face of second chip, 404A, using resin or paste, wherein the second chip is bonded face-up. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the device structure of Yang wherein the second chip is attached to the first chip using a resin or paste, in Masayuki et al. to provide a rigidly mounted device configuration.

16. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masayuki et al., as applied to Claims 1 – 4, 6, 9, 10, 13, and 14, and further in view of Moon (US 6,566,739 B2).

17. Regarding Claim 8, Masayuki et al. do not disclose a method for forming a conductive layer by ejecting a solution containing fine particles. Moon discloses a technique for forming

conductive traces (Figure 6), wherein a solution (81c) is ejected from a dispenser (93) (Col. 6, lines 16 – 26). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Moon in Masayuki et al. to provide an efficient means of forming conductive layer traces.

Conclusions

18. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone is **(571) 272-1658.** The Examiner can normally be reached on Monday through Friday from 8:30 AM to 5:00 PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732**. The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306**.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee

September 24, 2004